

27.7 CMOS Image Sensor with integrated 4Gb/s Camera Link Transmitter

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LVDS is a promising interface for machine-vision/automotive/medical CMOS image sensors, allowing low pin-count and over 500Mb/s data rates per pair of wires. The feasibility of image sensor with a single LVDS output yielding 60frames/s has been recently reported [1]. Some vision applications, however, require sensor data rates well above the capabilities of a single LVDS channel. Therefore, there is a demand for a wide LVDS interface, such as a camera link on an image sensor. Such a sensor is designed, manufactured, characterized, and is presented in this paper.

The sensor contains a pixel array, column ADCs at both top and bottom of the pixel array, data registers, and a camera-link transmitter (Fig. 27.7.1). A 5T shutter pixel (Fig. 27.7.2) is based on conventional photodiode and designed to increase sensitivity by utilizing charge transfer rather than charge share in the 5T shutter pixel [2]. A common reset switch is implemented to reduce the FPN and to provide the possibility of performing reset in "soft" mode with slightly lower kTC noise. The column ADC uses an auto-zeroing instead of a bulky capacitive DAC [2] for comparator offset removal. With the exception of a capacitor bank, the topology is fully differential, with the potential of capturing less substrate noise. The ADC core is a multistage high-speed comparator where each subsequent low-gain stage removes the offset of the previous stage.

Data from ADC is sampled into registers and is read out with a clock up to 100MHz via 6 parallel channels (this rate is proven in a separate chip). The internal data bus width is 48b; 24b is read at the bottom of the chip and the other 24b at the top. A camera-link transmitter serializes 48 CMOS-level signals into 8 LVDS outputs and also transmits the LVDS clock. The transmitter consists of a PLL, an 8-channel serializer, and 9 LVDS I/O pads. The PLL includes a phase detector, a charge pump, a filter, and a VCO; the design is based on the implementation reported in [3]. An essential part of the transmitter is the 8-channel serializer. In order to avoid the risks associated with multiplexing of signals at the VCO clock rate, the decision is made to use a sub-carrier clock generated in a divide-by-7 frequency divider which is part of the PLL. These waveforms (b1-b3) are generated synchronously from the outputs of simple dynamic D-FFs (Fig. 27.7.3.), and later splitted into 6 complementary delay-compensated decoder controls (b1-b3, b1n-b3n), buffered, and distributed over the array of the serializers. Figure 27.7.4 shows one channel of the serializer. It combines 7 differential NMOS current-steering circuits, each enabled with 3 decoding NMOS transistors in series. The differential pairs have a common load on 2 diode-connected PMOS transistors. The 7 differential signals to be multiplexed, d0/d0n through d6/d6n, are applied to the gates of the corresponding differential pairs. One pair is selected at a time to drive the load. Differential current-mode operation minimizes glitches (the adjacent branches compete for the load in the transition time), and low-resistance diode-connected loads insure high multiplexing rate and sharp edges of the output waveforms. LVDS clock is derived from the top bit in the divide-by-7 counter and passes a dummy serializer (the decoder inputs are enabled) to have the same delay as the rest of the data.

The transmitter realizes the conversion table in Fig. 27.7.5 to comply with one of the commercially available receivers. The line and the frame data syncs are built into the data by substitution of some imaging data (hex 00 and 01). One can notice 'all zeroes' in the conversion table for one column. In the commercial device, this column is taken to represent the dc-balance bit derived through a parity calculation. The sensor implements an alternative dc-balancing method. To equalize the representation of ones and zeroes in the transferred image, every second data bit passing an LVDS channel is inverted. In other implementations, this could be an inversion of the every second column data in the image, or/and the inversion of the every second bit in one byte. This dc-balancing technique is rather intuitive and uses statistical properties of the image, working as well in situations when the image is dark or saturated. The unscrambling of the data is done on the receiving end, both after the cable and after the receiver.

Outputs from the serializers are connected to pre-drivers to restore logic levels and then routed to LVDS pads. One LVDS pad is a standard current-steering bridge on 4 NMOS switches with a diagonal 100 Ω termination resistor. The mid point of the resistor is kept at the 1.25V required by the standard using a negative feedback that equalizes the current in the PMOS current source, pumping the bridge with the 8mA current sunk through an NMOS sink, in the way similar to [4]. The LVDS pad also has conventional clamps for ESD protection of the output and the internal nodes.

A microphotograph of the manufactured chip is presented in Fig. 27.7.7, and the measured parameters- in the table in Fig. 27.7.6. An evaluation board combines the image sensor, an FPGA for board-level controls and data multiplexing, a memory, a commercial deserializer, and 2 camera-link (input and output) connectors. The LVDS data is sent through a 3m cable and returned back to the board. The link was fully functional up to the rates of 80MHz demonstrating the transmission of the data with the data rate of up to 4 Gb/s.

Implementing this interface on a digital imaging sensor allows compact camera heads with the output data rates well exceeding the capabilities of any of the popular USB-2, IEEE1394, LVDS, or Gigabit Ethernet interfaces.

References:

- [1] N. Bock, et al., "A Wide-VGA CMOS Image Sensor with Global Shutter and Extended Dynamic Range," *Proc. of IEEE Workshop on CCDs and AIS, Karuizawa*, pp. 222-225, 2005.
- [2] A. Krymski, et al., "A 9-V/Lux-s 5000-Frames/s 512x512 CMOS Sensor," *IEEE Trans. on Electron Devices*, vol. 50, no. 1, pp. 136-141, Jan., 2003.
- [3] J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State. Circuits*, vol.31, no 11, pp.1723-1732, Nov., 1996.
- [4] A. Boni, et al., "LVDS I/O interface for Gb/s-per-Pin operation in 0.35-um CMOS," *IEEE J. Solid-State Circuits*, vol.36, no. 4, pp. 706-711, Apr., 2001.

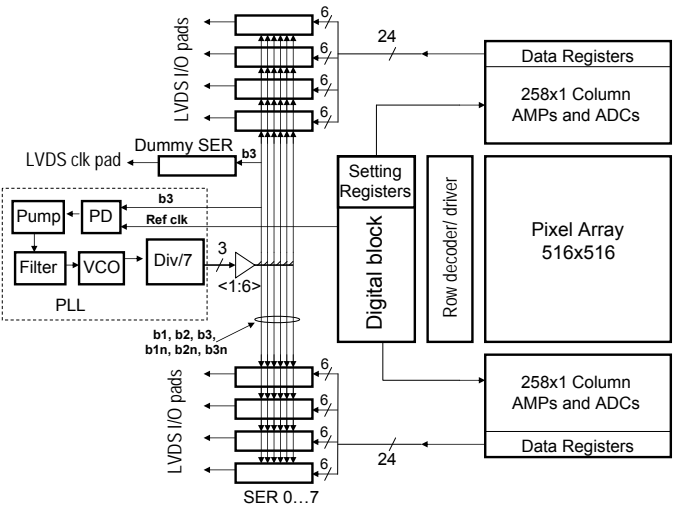


Figure 27.7.1: Sensor block-diagram.

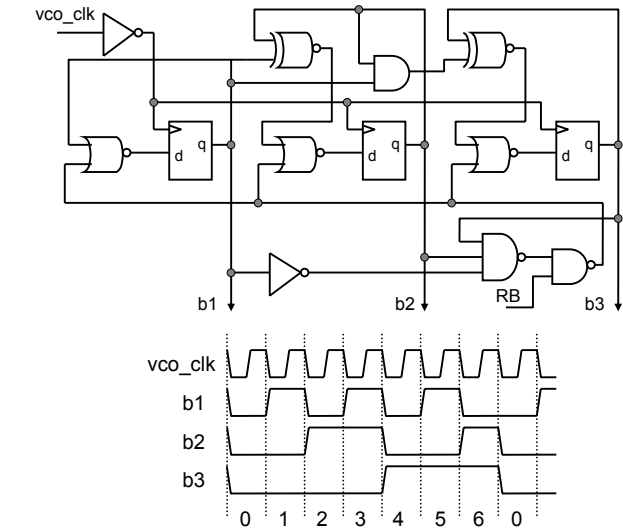


Figure 27.7.3: Generation of decoder waveforms b1-b3 in Div/7 block.

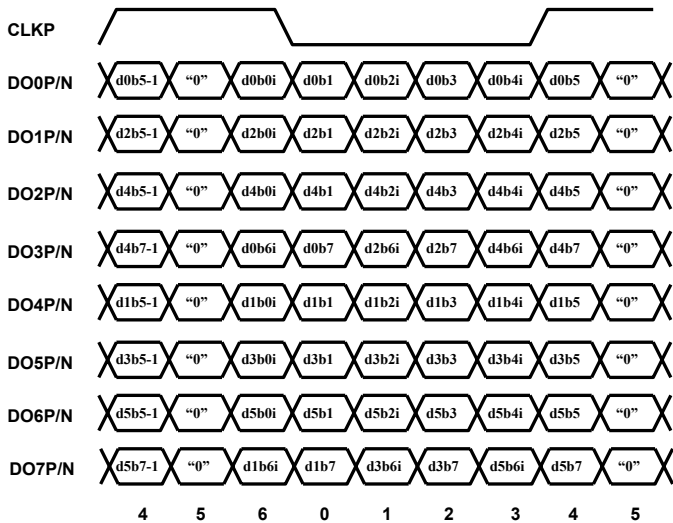


Figure 27.7.5: Serialization table: Suffix "i" denotes inverted bits.

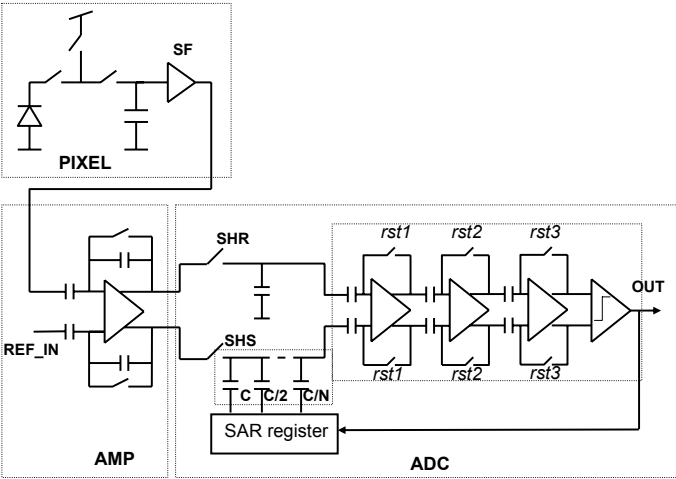


Figure 27.7.2: Pixel, column amp, and column ADC.

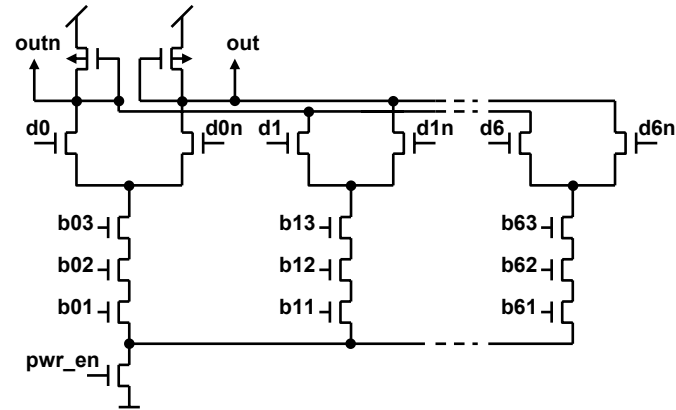


Figure 27.7.4: Serializer, multiplexing data d0..d6 using waveforms applied to b*1-b*3.

Technology	0.35μm 2P3M
Array format	516x514
Pixel	5T shutter pixel
Frame rate	>1,000frames/s
Clock rate	20 to 80MHz
Output interface	DS90CR484-compatible
Output	8 of 100Ω, 8mA LVDS drivers
Output clock	140 to 560MHz
Power	1.2W @3.3V
Responsivity	4.5V/Lux*s
Conversion gain	25μV/e
Noise	40e-
PRNU	1 % rms
DSNU	0.6% rms
Package	120-pin PGA

Figure 27.7.6: Specification summary.

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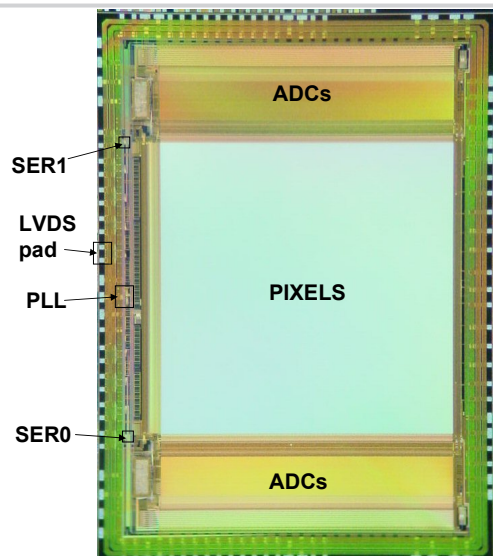


Figure 27.7.7. Chip micrograph.